REMARKS/ARGUMENTS

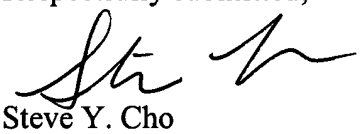
Claims 1-5, 7, 15 and 18 are allowed. Claims 6, 8 and 16-17 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicants respectfully traverse the rejection. Applicant notes that claim 6, 8, 16, and 17 were rejected for not using the proper Markush claim language, i.e., for reciting "a group consisting of." Claims 6, 8, 16, and 17 were amended to recite "from the group consisting of" in the amendment filed on July 5, 2006, which is enclosed for the Examiner's reference.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 206-467-9600.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

On July 5, 2006

TOWNSEND and TOWNSEND and CREW LLP

By: Sharyl Brown
Sharyl Brown

PATENT
Attorney Docket No.: 00939H-087400US
Client Ref. No.: P03H3001/US/cj

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

KIM et al.

Application No.: 10/749,909

Filed: December 30, 2003

For: METHOD FOR FABRICATING SEMICONDUCTOR DEVICE

Customer No.: 20350

Confirmation No. 1391

Examiner: George A. Goudreau

Technology Center/Art Unit: 1763

AMENDMENT

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action mailed April 7, 2006, please enter the following amendments and remarks:

Amendments to the Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) A method for forming a storage node contact of a semiconductor device, the method comprising:

depositing sequentially a conductive layer, a nitride layer and a polysilicon layer over a substrate, where at least one contact plug contacts the substrate;

patterning the polysilicon layer, the nitride layer and the conductive layer to form at least first and second conductive patterns, the patterned conductive layer defining the first and second conductive patterns, the patterned polysilicon and nitride layers defining first and second dual hard mask patterns provided over the first and second patterned conductive patterns, respectively, wherein the first and second conductive patterns define a first hole therebetween, the first hole being provided directly over the contact plug ;

forming an insulation layer over the first and second dual-hard masks and into the first hole; and

selectively etching the insulation layer to define a second hole and expose the contact plug.

2. (Previously Presented) The method as recited in claim 1, the method further including:

after forming the second hole, depositing an oxide layer at least along a profile of the second hole; and

thereafter, forming a spacer at sidewalls of each conductive pattern by etching the oxide layer through a blanket etch-back process.

3. (Original) The method as recited in claim 1, wherein the polysilicon layer is first deposited to a thickness ranging from about 1000 Å to about 2000 Å and is set to remain in a thickness ranging from about 300 Å to about 1000 Å after the bitline patterns are formed.

4. (Original) The method as recited in claim 1, wherein the nitride layer has a thickness ranging from about 900 Å to about 1500 Å.

5. (Previously Presented) The method as recited in claim 1, wherein the first and second conductive patterns are bit lines, gate electrodes, or metal wire.

6. (Currently Amended) The method as recited in claim 1, wherein the conductive layer is made of a material selected ~~from a group~~ from the group consisting of tungsten (W), titanium nitride (TiN), tungsten silicide (WSi_x), polysilicon (Poly-Si) and titanium (Ti).

7. (Original) The method as recited in claim 1, wherein the plug is formed with one of polysilicon and titanium nitride.

8. (Currently Amended) The method as recited in claim 1, the insulation layer is made of a material selected ~~from a group~~ from the group consisting of high density plasma (HDP) oxide, tetra-ethyl-ortho-silicate (TEOS), advanced planarization layer (APL) and spin-on-glass (SOG).

9. (Previously Presented) The method as recited in claim 1, wherein the insulation layer is etched using a line type photoresist pattern as an etch mask to define the second hole exposing the contact plug, wherein the photoresist pattern is removed after forming the second hole.

10. (Previously Presented) The method as recited in claim 9, wherein the photoresist pattern is formed using a light source of ArF or KrF.

11. (Previously Presented) The method as recited in claim 1, further comprising:

providing conductive material over the polysilicon layer, the conductive material filling the second hole; and

removing the at least conductive material and the polysilicon layer to form a planarized conductive structure that electrically couples to the contact plug, the conductive structure having an upper surface that is substantially planar to an upper surface of the nitride layer.

12. (Previously Presented) A method for fabricating a semiconductor device, the method comprising:

depositing sequentially a bit line conductive layer, a nitride layer and a polysilicon layer over a substrate in which a first plug is formed;

etching the polysilicon layer, the nitride layer and the bit line conductive layer to form at least first and second bit lines, the etched polysilicon and nitride layers defining first and second dual-structure mask patterns provided over the first and second bit lines, respectively ;

forming an insulation layer over the first and second dual-structure mask patterns and into a first hole defined between the first and second bit lines, the first hole being defined directly over the first plug; and

etching the insulation layer to form a second hole exposing the first plug.

13. (Previously Presented) The method as recited in claim 12, the method further including:

after forming the second hole, depositing an oxide layer at least along a profile of the second hole; and

thereafter, forming a sidewall spacer for each bit line by etching the oxide layer through a blanket etch-back process.

14. (Original) The method as recited in claim 12, wherein the polysilicon layer is first deposited to a thickness ranging from about 1000 Å to about 2000 Å and is set to remain in a thickness ranging from about 300 Å to about 1000 Å after the bit lines are formed.

15. (Original) The method as recited in claim 12, wherein the nitride layer has a thickness ranging from about 900 Å to about 1500 Å.

16. (Currently Amended) The method as recited in claim 12, wherein the conductive layer is made of a material selected ~~from a group~~ from the group consisting of tungsten (W), titanium nitride (TiN), tungsten silicide (WSi_x), polysilicon (Poly-Si) and titanium (Ti).

17. (Currently Amended) The method as recited in claim 12, the insulation layer is made of a material selected ~~from a group~~ from the group consisting of high density plasma (HDP) oxide, tetra-ethyl-ortho-silicate (TEOS), advanced planarization layer (APL) and spin-on-glass (SOG).

18. (Currently Amended) The method as recited in claim 12, further comprising:

depositing a plug material into the second hole and over ~~the~~ the exposed first plug; and

removing at least the plug material and the polysilicon layer to form at least one second plug that electrically couples the first plug,

wherein the plug material and the polysilicon layer are removed until an upper surface of the nitride layer and is substantially planar to an upper surface of the second plug.

REMARKS/ARGUMENTS

Claims 1-18 are pending. Claims 1, 6, 8, and 16-17 have been amended. No claim has been added or canceled. No new matter has been added.

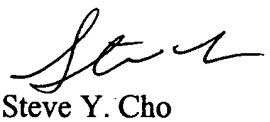
Claims 1-11 and 16-18 were rejected under 35 U.S.C. § 112, second paragraph. Claims 1, 6, 8, 16, 17, and 18 have been amended in response to the rejection. Applicants thank the Examiner for allowing claims 12-14.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 650-326-2400.

Respectfully submitted,



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